

REMARKS

Claims 1 to 8, 10 to 18 and 20 to 28 and 30 to 33 are pending this application of which claims 1, 11 and 21 are the independent claims. Favorable reconsideration and further examination are respectfully requested.

Initially, Applicants thank Examiner Thompson for taking the time to conduct a personal interview on Monday, March 1, 2004 to discuss these rejections.

The Examiner rejected claims 1 to 8, 10 to 18 and 20 to 30 under §112, first paragraph, for allegedly failing to enable embedding a computer instruction representing a combinatorial element. During the interview, the Examiner indicated that she would remove the §112 rejection in view of the arguments presented in the interview. The Examiner also agreed not to make the next action final (assuming a next action is necessary).

Claims 1 to 8, 10 to 18 and 20 to 30 were rejected under 35 U.S.C. § 102 over Rostoker et al. (U.S. Patent No. 5,544,067). As shown above, Applicants have amended the claims to define the invention more clearly. In view of these amendments, withdrawal of the art rejection is respectfully requested.

Claim 1 is directed to a method of generating a logic design for use in designing an integrated circuit (IC). The method includes embedding a computer instruction within a two-dimensional schematic representation of the logic design to produce a unified database representation of the logic design. The computer instruction is devoid of declarations. The two-dimensional schematic representation includes a set of Register Transfer Diagrams (RTD).

The applied art is not understood to disclose or suggest the foregoing features of claim 1. In particular, Rostoker does not disclose or suggest embedding a computer instruction that is devoid of declarations in a two-dimensional schematic representation of a logic design.

As understood by the Applicants, the Examiner indicated during the interview that Rostoker suggests embedding an instruction within a functional block in order to represent a lower-level functional block (see column 27, lines 19 to 42 of Rostoker). Rostoker, however, does not disclose or suggest the content of such an instruction. Accordingly, Rostoker cannot possibly disclose or suggest that the instruction is devoid of declarations.

Claims 1 to 8, 10 to 18, 20 to 28 and 30 were also rejected under 35 U.S.C. § 102(b) over the Mentor Graphics data sheets (HDL Design data sheet and Renoir with HDL2Graphics data sheet).

The Mentor Graphics datasheets indicate that computer instructions and two-dimensional schematic representations may be used to design an IC, but the data sheets do not disclose or suggest that the computer instructions of a combinatorial block are embedded into the two-dimensional representations. In fact, the data sheets show each of the representations in separate display windows. For example, the first page of the HDL Design data sheet shows one display window for code and a second display window for combinatorial blocks. In another example, the Renoir with HDL2Graphics data sheet shows different display.

Furthermore, the data sheets do not disclose or suggest use of a computer instruction that is devoid of declarations. Accordingly, Applicants respectfully request withdrawal of this rejection.

For at least the foregoing remarks, Applicants believe that claim 1 is allowable.

Claims 11 and 21 roughly correspond to claim 1. Accordingly, claims 11 and 21 are believed to be allowable for at least the same reasons noted above with respect to claim 1.

The dependent claims each incorporate by reference the patentable features noted above. Accordingly, the dependent claims are also believed to be allowable.

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

In view of the foregoing amendments and remarks, Applicants submit that the entire application is now in condition for allowance. Such action is respectfully requested at the Examiner's earliest convenience.

Applicants : William R. Wheeler et al.  
Serial No. : 09/942,102  
Filed : August 29, 2001  
Page : 11 of 11

Attorney's Docket No.: 10559-595001  
Intel Docket: P12879

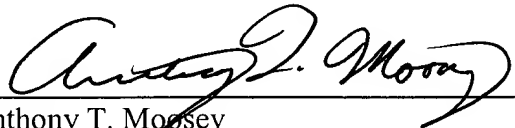
Applicants' attorney can be reached by telephone at the number shown below.

No fee is believed to be due for this Response; however, if any fees are due, please apply such fees to Deposit Account No. 06-1050 referencing Attorney Docket 10559-595001.

Respectfully submitted,

Date: \_\_\_\_\_

3/16/2004

  
\_\_\_\_\_  
Anthony T. Moosey  
Reg. No. 55,773

Attorneys for Intel  
Fish & Richardson P.C.  
225 Franklin Street  
Boston, MA 02110-2804  
Telephone: (617) 542-5070  
Facsimile: (617) 542-8906